CLAIMS

What is claimed is:

1. An integrated circuit, comprising logic circuits connected to a plurality of scan chains and self-test circuits for testing said logic circuits, said self-test circuits comprising:

a pseudo random pattern generator for generating at least one flat pseudo random pattern;

weighting circuits for providing a selectable weight set to said flat pseudo random patterns;

a storage element associated with each of the weighting pattern generators receipt of a random pattern from the associated random pattern generator; and

a selection circuit for individually addressing each of the storage elements for providing said weighted pseudo random pattern to said scan chains independently of one another for scanning said weighted pattern to said logic circuits to enable provision of different weights to the storage elements.

2. An integrated circuit as recited in claim 1, wherein said weighting circuit comprises a weight generating circuit and a weight selecting circuit.

3. The integrated circuit as recited in claim 1, wherein said weighting circuit includes means for receiving a weighting instruction from an external source to said integrated circuit.

4. The integrated circuit as recited in claim 1, wherein said storage elements are each a first stage of an associated scan chain.

5. The integrated circuit as recited in claim 4, wherein said pseudo random pattern generator and said weighting patterns, receipts pattern and weighting instructions from a tester internal to said integrated circuit.

6. The integrated circuit as recited in claim 4, wherein said weighting instruction is generated by a tester external to said integrated circuit.

7. The integrated circuit as recited in claim 4, further comprising a memory or register array wherein at least a portion of said weighting instruction is stored in said memory array.

8. A method of testing an integrated circuit, comprising logic circuits connected to scan chains and self-test circuits on said integrated circuit for testing said logic circuits, the method comprising:

a) generating a pseudo random pattern;

b) providing a weight to said pseudo random pattern; and

c) selectively providing said weighted pseudo random pattern to at least one but not all the scan chains for scanning said weighted pattern to the logic circuits.

9. The method as recited in claim 8, wherein said weighted pseudo random pattern is introduced to a portion but not all of said at least one scan chain.